REPLACEMENT CLAIMS

1. (Amended) A method of forming a flash memory cell, comprising:

forming a tunnel oxide on a substrate;

forming a first conductor layer over said tunnel oxide;

forming an insulating layer over said first conductor layer, said insulating layer comprising a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer, wherein said second oxide layer is formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes;

forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate on opposite side of said stacked gate structure, thereby forming at least one memory cell.

16. (Amended) A method of forming an ONO insulating structure, comprising:

depositing a first oxide layer over an integrated circuit structure;

depositing a nitride layer over said first oxide layer; and

growing a second oxide layer over said nitride layer wherein said second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer.

31. (Amended) A method of forming a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells being formed by the acts of:

forming a tunnel oxide on a substrate;

forming a first conductor layer over said tunnel oxide;

forming an insulating layer over said first conductor layer, said insulating layer comprising a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer, wherein said second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen at a temperature of less than about 900°C;

forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate, thereby forming at least one memory cell.